**module RAM\_16x8\_ex1 (clk, addr, RW, i\_data, o\_data);**

**input clk;**

**input [3:0] addr;**

**input RW;**

**input [7:0] i\_data;**

**output reg[7:0] o\_data;**

**reg [7:0] Mem [0:15];**

**always @ (posedge clk)**

**if (RW)**

**Mem[addr] <= i\_data;**

**else**

**o\_data <= Mem[addr];**

**endmodule**

**module RAM\_16x8\_ex1\_testbench();**

**reg clk;**

**reg [3:0] address;**

**reg RW\_enable;**

**reg [7:0] data\_in;**

**wire [7:0] data\_out;**

**RAM\_16x8\_ex1 ram1 (**

**.clk(clk),**

**.addr(address),**

**.RW(RW\_enable),**

**.i\_data(data\_in),**

**.o\_data(data\_out));**

**initial begin**

**$display("RAM test bench.");**

**clk = 1;**

**#10 RW\_enable = 1;**

**address = 0;**

**data\_in = 8'haa; //1010 1010**

**#10 address = 7;**

**data\_in = 8'h55; //0101 0101**

**#10 RW\_enable = 0;**

**#10 $display($time, " Mem[%d] = %h", address, data\_out);**

**#10 address = 0;**

**#10 $display($time, " Mem[%d] = %h", address, data\_out);**

**#10 address = 1;**

**#10 $display($time, " Mem[%d] = %h", address, data\_out);**

**#10 RW\_enable = 1;**

**address = 1;**

**data\_in = 8'h2a; //0010 1010**

**#10 RW\_enable = 0;**

**#10 $display($time, " Mem[%d] = %h", address, data\_out);**

**#200 $finish;**

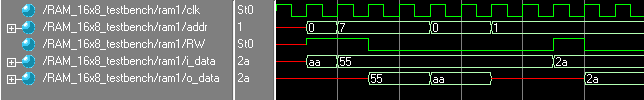
**end**

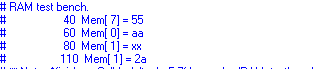
**always begin**

**#5 clk = ~clk;**

**end**

**endmodule**

****

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